TITLE OF THE INVENTION

Multi-Level Pulse Width Modulation in Digital System

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. §119(e) of U.S. Provisional Patent Application No. 60/451,394 filed March 4, 2003.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

--Not Applicable--

BACKGROUND OF THE INVENTION

The invention relates to the field of digital systems employing pulse width modulation (PWM), and in particular to digital audio systems employing PWM to generate audio signals from corresponding digital signals.

The current trend in the audio field is for digital recording and retrieval of audio source material, rather than analog recording and retrieval as practiced for so long in the history of the field. As a result, digital audio amplifier systems suitable for direct processing of digital sources have been of great interest to the consumer electronics industry over the past few years. Digital audio amplifier systems eliminate the need for an intermediate digital-to-analog conversion, and thereby offer improved sound quality.

A typical prior art digital audio amplifier system for direct processing of a digital audio signal includes an interpolator stage which employs inter-sample estimating to up-sample the digitally-encoded audio stream to a rate several times the original sampling rate; a pulse width modulation (PWM)

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converter stage that converts digital samples to fixed-amplitude pulses with pulse widths corresponding to sample values; and a power-switching stage controlled by the PWM pulse signal. The output of the power-switching stage is fed to a low-pass filter such as an inductor-capacitor (LC) filter, and the output of the filter is fed to one or more loudspeakers.

The purpose of the interpolator circuit is to increase the frequencies of sampling-induced frequency components (such as aliasing components) to facilitate attenuation of such components by the low-pass filter and thereby render them substantially inaudible at the loudspeaker. However, there are practical limits to the resolution or dynamic range of the amplifier that are reached at high sampling frequencies. These limits arise from the limited switching speed of the power output switches. For example, for a digital signal having 10-bit quantization and a 48 KHz sampling rate up-sampled by a factor of 8, faithful reproduction would require switching speeds on the order of 2-3 ns. This is generally not feasible for present high-power switching components, and in any event might result in an unfavorable cost/performance tradeoff.

Accordingly, it is also common to include a noise shaper circuit in current digital audio systems to convert the high-resolution data from the interpolator stage to lower-resolution data. For example, a 16-bit quantized digital signal might be reduced to 6 to 8 bits of quantization at the higher up-sampled rate, to better match the characteristics of the digital signal with the switching speed of the power output switches.

The up-sampling of the digital signal tends to offset some of the loss of resolution from the noise shaper. For example, up-sampling by a factor of 8 can theoretically offset a 3-bit loss of resolution from the noise shaper. However, the overall resolution of the digital audio system is still undesirably

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limited, especially in comparison to the 16-bit resolution of modern compact disc (CD) systems. It would be desirable to provide for greater resolution in digital audio systems without requiring very-high-speed switching devices.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, methods and apparatus providing multi-level pulse width modulation (multi-level PWM) are disclosed. An input signal is converted into an N-level PWM signal which conceptually is a composite signal consisting of the sum of a fixed amplitude PWM pulse with variable pulse width Tw within a sampling cycle and a pulse with width equal to the maximum pulse width Twmax of the PWM pulse within the sampling cycle and amplitude equal to n times the amplitude of the fixed-amplitude PWM pulse, where n can be any number from 0 to N-1 and Twmin is the minimum width of the said PWM pulse within the sampling cycle such that the value of (Tw + n*Twmax)/Twmin for the sampling cycle equals the value of the data sample of the input signal in that sampling cycle. It can be seen that a system employing N-level PWM will have N times the resolution of a corresponding system employing PWM.

The multi-level PWM can be applied to digital amplification in high fidelity audio systems to address the limitation in resolution of existing PWM-based digital audio system. The multi-level PWM can also be adapted to control the output of other types of systems with similar improvement in resolution.

In general, apparatus is disclosed for controlling switching circuitry being operative to generate an analog output from a digital signal, the digital signal carrying multi-bit values at a sampling rate. The analog output may be audio sound outputs or other types of outputs.

The digital signal also includes first and second digital sub-signals carrying, respectively, the least-significant and

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most-significant components of the multi-bit values carried by the digital signal.

The apparatus includes switch control circuitry that generates a set of control signals to control the electrical outputs of the switching circuitry. The control signals collectively include a pulse width modulated signal based on the first digital sub-signal and multi-channel and/or multi-level control signals based on the second digital sub-signal. By including the multi-channel and/or multi-level control, the apparatus can provide additional resolution in the analog output than provided by apparatus that employs only pulse width modulation. The resolution increases by a factor of n, where n is equal to the aggregate total of the number of different levels available in each channel.

Three embodiments of the apparatus are shown. In a first embodiment, the analog output is generated from a multi-level electrical signal including a pulse width modulated component and a multi-level component. The switching circuitry includes a number of switches each providing one of the levels of the multi-level electrical signal in response to assertion of a corresponding control signal. A PWM converter generates a pulse width modulated signal and a maximum-width-pulse signal, the pulse width modulated signal being based on the first digital sub-signal, the maximum-width-pulse signal establishing the maximum permissible pulse duration in a sampling cycle for the pulse width modulated signal. The switch control circuitry includes a level selector that asserts each control signal based on the PWM converter's signals and the second digital sub-signal. In this embodiment, respective sources of all the levels of the multiple levels of the electrical signal are required, such as a set of power supplies each providing a different voltage level.

In a second embodiment, the analog output is generated by additively combining a plurality of analog component outputs

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generated from corresponding electrical signals from separate channels (the term "channel" being used in a generic sense independent of other channelization that may occur in the system, such as traditional stereo or quadraphonic separation). In the case of an audio analog output, the analog component outputs are audio component outputs from separate loudspeakers, which are additively combined in a transmission medium such as air. The switching circuitry includes a number of switches that each generates a predetermined level on the electrical signal of the channel in response to a corresponding control signal. A PWM converter generates a pulse width modulated signal and a maximum-width-pulse signal, the pulse width modulated signal being based on the first digital sub-signal, the maximum-width-pulse signal establishing the maximum permissible pulse duration in a sampling cycle for the pulse width modulated signal. The switch control circuitry includes an encoder that asserts different numbers of the control signals based on the value of the second digital sub-signal. In one channel the control signal for the switching circuitry consists of the pulse width modulated signal. In the other channels, the control signals consist of the control signals from the encoder and the maximum-width-pulse signal from the PWM converter. In this embodiment, only a single level is required to generate each electrical signal, and thus this embodiment can operate from a single power supply.

The third embodiment employs both multi-level electrical signals and multiple channels whose outputs are additively combined. Additionally, filters are utilized to separate the digital audio signal into separate frequency bands, so that the digital-to-analog circuitry for each band can be optimized. A higher frequency band can achieve a certain resolution using the multiple-channel approach, whereas fewer channels (e.g., only one) are needed to obtain the same resolution in lower frequency bands.

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Other aspects, features, and advantages of the present invention will be apparent from the Detailed Description of the Invention that follows.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The invention will be more fully understood by reference to the following Detailed Description of the Invention in conjunction with the Drawing, of which:

Figure 1 is a block schematic diagram showing the principal components of a typical prior art PWM based digital audio power amplifier;

Figure 2 is a block schematic diagram of a digital audio system employing multi-level PWM in a first fashion in accordance the present invention;

Figure 3 is a timing diagram illustrating the operation of the digital audio system of Figure 2;

Figure 4 is a block schematic diagram of a digital audio system employing multi-level PWM in a second fashion in accordance with the present invention;

Figure 5 (consisting of Figures 5a and 5b) is a block schematic diagram of a digital audio system employing multi-level PWM in a third fashion in accordance with the present invention; and

Figure 6 is a timing diagram illustrating the operation of the digital audio system of Figure 5.

DETAILED DESCRIPTION OF THE INVENTION

The disclosure of U.S. Provisional Patent Application No. 60/451,394 filed March 4, 2003, is hereby incorporated by reference.

A typical prior art digital audio amplifier system for direct processing of a digital audio signal is shown in Figure 1. The amplifier includes a serial interface 100, interpolator 110,

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noise shaper 120, pulse width modulation (PWM) converter 130, and a switching stage 140. The output of the switching stage 140 feeds an inductor-capacitor (L-C) low-pass filter 150 which in turn feeds a loudspeaker 160. The serial interface 100 converts an M-bit serial digital input data stream at a sampling rate Fs into an M-bit parallel data stream 101 at the same sampling rate. The interpolator stage 110 up-samples the M-bit parallel data 101 at a rate X times the original sampling rate of Fs, i.e. X*Fs (typically over 300KHz), by estimating the required intermediate values between two consecutive data samples. This enables attenuation of the sampling frequency components by the low pass filter 150 to render such frequency components substantially inaudible at the loudspeaker 160.

The noise shaper stage 120 converts the high resolution data signal 111 from the interpolator 110 to a coarse-quantized data signal 121 with reduced resolution of Q bits (e.g. 6-8 bits) at the sampling rate of X*Fs to be compatible with the switching speed of the switching devices in the switching stage 140, as explained above. The PWM converter 130 converts the Q-bit coarse-quantized data signal 121 to a PWM signal 131. In one typical implementation, the PWM converter compares each input Q-bit data sample with the output of a counter clocked by a bit-clock running at $X*(2^Q)*Fs$, which is typically the fastest clock in the system and defines the minimum pulse width of the PWM signal 131. The switching stage 140 typically consists of high speed power MOSFET switches in H-bridge configuration operated in the cut-off or saturation region. The switches are controlled by the PWM signal 131 to transfer power from a power supply (not shown) through the L-C low pass filter 150 to the loudspeaker 160.

The amplifier in Figure 1 can be implemented digitally from the serial interface 100 through the switching stage 140 without requiring any intermediate digital to analog conversion, and

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theoretically will have less noise and distortion and better performance than other approaches. As described above, the practical resolution or dynamic range of such an amplifier is limited by the switching speed of the power output switches in switching stage 140. For this reason, present PWM based audio power amplifiers generally employ some sort of noise shaping technique (represented in Figure 1 by the noise shaper 120) to reduce the resolution of each sample of the output PWM signal. While this reduced resolution is more compatible with existing switching devices, it also undesirably limits performance.

Figure 2 shows a first embodiment of a multi-level PWM technique for obtaining improved performance over digital amplifiers of the type depicted in Figure 1. The serial interface 300 and interpolator 310 operate in the same manner as their counterparts in the amplifier of Figure 1 to produce an M-bit up-sampled data stream 311 which is assumed to be unsigned (a signed data can be converted to an unsigned data by adding an offset to it). Each M-bit data sample is divided into two data samples, one sample having the K least significant bits and one sample having the J most significant bits, where M = J + K. The streams of K-bit samples and J-bit samples respectively form sub-signals 312 and 313 of the M-bit signal 311.

A noise shaper 320 converts the high resolution K-bit data stream 312 to a coarse-quantized data stream 321 with reduced resolution of Q bits at the up-sampled rate of X*Fs. A PWM converter 330 converts the Q-bit coarse-quantized data stream 321 into a PWM signal Tw 331. As shown, the PWM converter 330 also generates a signal Twmax 332 having a fixed pulse width equal to the maximum pulse width of Tw 331 in the sampling cycle, which is described in more detail below.

The signals Tw 331 and Twmax 332 are provided to a level selector 340 along with the J-bit data stream 313 from the interpolator 310. These signals are used by the level selector

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340 to control a set of switches in an output switching stage 350 to switch among 2^J+1 voltage levels (including the zero voltage level) to generate a multi-level PWM signal 351. The multi-level PWM signal 351 is supplied to a low-pass filter 360 which drives a loudspeaker 370. The voltage levels selectable by the switching output stage 350 can have positive or negative polarity as shown and have amplitudes equal to respective multiples of a predetermined fixed reference voltage level "V".

The level selector 340 controls the set of switches in the output switching stage 350 to switch among the levels in a manner tending to minimize the power required to operate the amplifier and the DC current flowing through the loudspeaker 370. In particular, during each sampling cycle the level selector 340 generates control signal 341 to select among the output voltages provided by the switching stage 350. The generation of the control signals occurs in the manner described below, which is illustrated for the special case of J = 2 in Figure 3:

1. During the initial portion of each sampling cycle as established by the variable-width pulse of Tw 331, a voltage is selected that is one level higher (more positive) than a base voltage level for the cycle as established by the value of the J-bit signal 313 (described below). Thus, if the base voltage level is +2V, the level +3V is selected during the initial portion of the cycle.

2. During the next portion of the cycle, the base voltage level for the cycle is selected. As indicated above, the base voltage level is established by the J-bit value. A binary value of zero corresponds to the lowest (i.e. most negative) voltage level (i.e., $-2^{(J-1)}V$), and successively greater binary values correspond to successively higher voltages. This

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portion of the cycle lasts until the end of the maximum pulse duration as established by the signal Twmax 332.

3. During the remainder portion of each sampling cycle that extends beyond the maximum pulse duration as established by Twmax, the zero voltage level is selected. The zero value is also selected in the absence of the input signal 301.

It can be seen that a supply of P different voltages is needed under the scheme of Figure 2 to produce P-level PWM signals. This requires the use of a multi-output power supply or a set of single-output power supplies each providing a different output voltage.

Figure 4 shows a second embodiment of a multi-level PWM technique that requires only one supply voltage. The operations of the serial interface 400, interpolator 410, noise shaper 420, and PWM converter 430 are the same as the corresponding elements in the amplifier of Figure 2. The M-bit data stream 411 is assumed to be unsigned (a signed data can be converted to an unsigned data by adding an offset to it). An encoder 450 converts the J-bit values 413 to a pattern of "ON" values on 2^J-1 control lines 451, such that the total number of control lines 451 turned on at any given time corresponds to the binary number represented by the J-bit data 413 at that time. For the above case of J = 2, this encoding could be realized as follows:

J	# of control lines ON
00	0
01	1
10	2
11	3

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The control lines 451 and the Twmax signal 432 from the PWM converter 430 control each of a set of switches 460 to switch between a single voltage level V and the zero voltage level, such that a maximum-width pulse 461 (width equal to Twmax 432) is outputted to each low pass filter 462 for which the corresponding control line 451 is ON in a sampling cycle. The filtered signal is provided to the corresponding loudspeaker 463.

Additionally, the Tw signal 431 from the PWM converter 430 is provided to a set of switch 440 that also switches between the voltage level V and the zero voltage level. In this case, a variable-width pulse stream at the sampling rate of X*Fs is outputted to a low pass filter 442 and the filtered signal is provided to a loudspeaker 443.

The separate acoustic signals from the speakers 443 and 463 are mixed additively in the sound-carrying medium, typically air, to produce the same acoustic effect as when a single low pass filter and loudspeaker are used to output a multi-level PWM signal such as described above with reference to Figures 2 and 3. Thus, the separate signals constitute component signals of the overall acoustic audio signal. It can be seen that P output channels are required to achieve the same effect as the one channel technique of Figures 2 and 3 producing P-level PWM signals. However, only one power supply voltage V is required, which in some applications may be preferable to requiring multiple supply voltages.

In addition to the amplifiers of Figures 2 and 4, amplifiers using a hybrid approach can also be constructed. That is, a multi-level PWM amplifier can be made using multiple supply voltages and multiple channels. An example is presented below in connection with the use of frequency division (or crossover separation) to make more efficient use of multiple loudspeakers.

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Often, any single loudspeaker is not able to faithfully reproduce the whole spectrum of audio frequencies. Some types of loudspeakers are better at reproducing lower frequencies, while other types of loudspeakers are better at reproducing higher frequencies. Traditionally, high fidelity audio systems employ analog band filters or crossover networks to divide the amplified audio signal into multiple signals in different frequency bands. The different signals are fed to different loudspeakers, where each loudspeaker is tailored for reproducing sounds of the frequency band of the signal it receives. For digital audio systems employing a single-output amplifier such as the amplifier of Figure 2, it may be practical for the loudspeaker system to include a number of loudspeakers and a crossover network. However, for systems employing a multiple-output technique such as shown in Figure 4, the number of loudspeakers that is required may be impracticably high, especially the large loudspeakers generally required for the low frequency band.

To address this issue, it is noted that a low frequency signal can be sampled at a lower rate than a high frequency signal to produce the same resolution. For example, sampling a 3 KHz signal at 96 KHz and a 12 KHz signal at 384 KHz provide the same resolution. Also, sampling a 3 KHz signal at 384 KHz shall, theoretically, provide 4 times greater resolution than sampling a 12 KHz signal at the same 384 KHz. Hence, if the digital signal is divided into a high frequency band and a low frequency band with an appropriate crossover frequency, such as 3 KHz, and the two signals are processed separately but in the same way in an amplifier employing the multiple-output approach, the outputs of the low frequency band will have about 4 times the resolution of the outputs of the high frequency band. As a result, one quarter of the number of loudspeakers or channels employed in the high frequency band can be employed in the low frequency band so that the outputs of both bands will have the same effective

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resolution. Those skilled in the art will appreciate that the number of frequency bands may be different in different applications.

Figure 5 shows an example of a system employing such frequency division, along with the multi-channel, multi-voltage hybrid approach mentioned above. The system of Figure 5 employs a band-separating filter 510 to divide the M-bit parallel data signal 501 into a high frequency M-bit signal 511 and a low frequency M-bit signal 515. The crossover frequency of the band-separating filter 510 in this two-way frequency division is 3 KHz. The system employs four channels and 8 non-zero voltage levels for the high frequency M-bit signal 511, resulting in a resolution of 32 times (or 5 bits more) the resolution that can be provided by just employing PWM using similar-speed switching devices.

The low frequency M-bit signal 515 can be processed in the manner shown in Figure 2 employing 8 nonzero voltage levels, i.e., using a single-output, multiple-voltage approach to achieve the same effective resolution as its high frequency counterpart as explained in above.

The high-frequency M-bit signal 511 is processed in the hybrid manner discussed above, i.e., using multiple channels as well as multiple voltages in each channel. The high frequency M-bit signal 511 which is assumed to be unsigned (a signed data can be converted to an unsigned data by adding an offset to it) will go through the interpolator 520 which up-samples the M-bit data 511 at a rate X times the original input sampling rate of Fs i.e. X*Fs to produce the M-bit data 521. In this example X = 8. Each M-bit data sample 521 is split into two data samples, one sample of J bits 523 (in this example J = 5) and one sample of K bits 522 where M = J + K. The J-bit sample 523 represents the most significant bits of the original M-bit data sample 521 whereas

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the K-bit sample 522 represents the least significant bits of the original M-bit data sample 521.

The noise shaper 530 will convert the high resolution K-bit data 522 to a coarse-quantized data 531 with reduced resolution of Q bits at the same sampling rate of 8*Fs. In this example Q = 8. A PWM converter 540 will convert the 8-bit coarse-quantized data 531 directly to a PWM signal and will output the PWM pulse with width Tw 541 and the maximum pulse width Twmax 542 of the PWM signal to the level selector 551.

An encoder 580 receives the 5-bit most significant data signal 523 and uses this signal to control the states of 31 control lines in four groups 581, 582, 583 and 584. These control lines are shown as numbered from #1 to #31. Each of these control lines is turned ON whenever the binary number represented by the 5-bit data 523 is greater than or equal to the number associated with the control line. For example, if a 5-bit data value of '01000' is provided to the encoder 580, control lines #1 to #8 are ON and the rest of the control lines are OFF. The PWM output signal Tw 541 and the 31 control lines from the encoder 580 together represent a 32-level PWM signal.

During each sampling cycle the level selector 552, 553 or 554 generates control signals to select among the 9 output voltage levels (including the zero voltage level) provided by the switching stage 562, 563 or 564 respectively. The selection of output voltage levels occurs in the manner described below:

1. During the initial portion of each sampling cycle established by the signal Twmax 542, the output voltage level or base voltage level for the cycle is selected according to the number of control lines that is ON in the group (582, 583 or 584 respectively) connected to the level selector. No control lines ON corresponds to the lowest voltage level (i.e., -4V), and

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successively greater number of control lines ON corresponds to successively higher voltages.

2. During the remainder portion of each sampling cycle that extends beyond the maximum pulse duration as established by Twmax, the zero voltage level is selected. The zero value is also selected in the absence of the input signal 511.

Level selector 551 differs from the other level selectors because it receives the signal Tw 541 in addition to control lines in group 581 from the encoder 580 and the signal Twmax 542. Level selector 551 thus operates in the same manner described above for level selector 340 of Figure 2 with the number of control lines in group 581 ON corresponding to the value of the J-bit signal 313 of Figure 2, i.e., no control line ON to level selector 551 corresponds to J-bit value equal to zero for the level selector 340. In particular, each cycle of the pulse signal outputted by the switching stage 561 has a variable-width initial portion that is one level higher than the next portion of the cycle as determined by the signal Tw 541. In contrast, the switching stages 562, 563 and 564 output only maximum-width pulses (width equal to Twmax 542).

As shown in Figure 5, the control lines from the encoder 580 are grouped into four groups as follows:

1. Group 581 includes lines #4, #8, #12, #16, #20, #24, #28;
2. Group 582 includes lines #1, #5, #9, #13, #17, #21, #25, #29;
3. Group 583 includes lines #2, #6, #10, #14, #18, #22, #26, #30;
4. Group 584 includes lines #3, #7, #11, #15, #19, #23, #27, #31.

Those skilled in the art will appreciate that the number of control lines in a group and the way to group the control lines

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from the encoder 580 is a matter of choice as is appropriate for the specific system to which the present invention is put to use.

Because of the interleaved nature of the grouping of the control lines, each successively higher value of the 5-bit signal 523 results in increasing the base level in a successively different channel rather than increasing the base level in only one channel at a time. This helps to distribute power evenly among the different loudspeakers 571, 572, 573 and 574. This operation is explained in more detail with respect to Figure 6 below.

Figure 6 illustrates the output signals to the high-frequency loudspeakers 571, 572, 573 and 574 of Figure 5 for a particular sampled analog signal. The additive effect of the four channels is depicted as a pulse waveform superimposed on the analog signal. The incremental increasing of base level across the channels is shown. For example, in the second cycle, the base level is increased by one step for the channel containing switches 564. In the third cycle, the base level is increased in the channels containing switches 561 and 562, etc.

The system of Figure 5 produces the same acoustic effect as though an equivalent 32-level PWM signal were provided to a single equivalent L-C low pass filter and loudspeaker. This is equivalent to 5 additional bits of resolution. With the 8-bit resolution of the signal from the noise shapers 530 and the 3-bit increase in resolution created by the interpolators 520, the overall system resolution is 5 + 8 + 3 = 16 bits. In general, using Y channels and a Z-voltage-level power supply to the full extent yield the equivalent of a (Y*Z)-level PWM signal.

It should be noted that it is desirable to equalize the respective outputs of the one-channel low-frequency band and the four-channel high-frequency band. This can be accomplished, for example, by making the four high frequency loudspeakers 571, 572, 573 and 574 with equal impedance and making the low frequency

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loudspeaker 599 with an impedance one quarter of that of each high frequency loudspeaker.

A variation of the multi-voltage and multi-channel scheme is to have a dedicated channel for the PWM signal so that the output of this PWM channel will swing between a positive and negative voltage level instead of between two adjacent levels and become zero only if there is no input signal or during the remainder portion of each sampling cycle that extends beyond the maximum pulse duration as established by Twmax. This PWM channel is still count as single level although it has an extra zero level. The other channels will be multi-level just like the above channels that contain the level selectors 552, 553 and 554. However, the output of the PWM channel will have to be equalized with those of the other channels.

Since all of the above schemes are based on unsigned data sample, therefore when the output of a channel is multi-level and swings between positive and negative voltage levels, the PWM pulse appears to be near the end of the sampling cycle when the output is negative. Usually the position of the PWM pulse within a sampling cycle is not significant but if it is important for a specific application, the logic of the level selector of the multiple voltage levels schemes will need the following changes to correct it. The PWM converter stage will need to output an extra Tx signal with pulse width equal to (Twmax - Tw) at the beginning of a sampling cycle. Whenever the value of the J-bit data input to the level selector or encoder in FIG. 2 or FIG. 5 falls below a threshold indicating a negative output level, the level selector that normally use the Tw signal will use the Tx signal instead to control the set of switches such that the voltage level outputted during Twmax but not during Tx will be one voltage level higher than during Tx.

All the electronic circuitry of the digital audio system of the present invention can be incorporated in an IC chip or chip

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set and therefore the physical size of the system will be mainly determined by the size of its power supply and L-C low pass filters.

For systems employing multiple output channels such as in Figures 4 and 5, it may be convenient to place the entire system including all the loudspeakers in one enclosure to eliminate the necessity of running many wires from the outputs to the loudspeakers. Also, each channel output can be driven by a separate power supply, each based on the same reference voltage level as the others. In this way, a number of smaller power supplies, each dedicated to one output and not affected by the other outputs, can be used to produce a large overall system output power, such as 500 watts for example.

For systems employing multiple voltage levels such as in Figures 2 and 5, each switching output stage can be configured with switches in a multiple H-bridge configuration so that the load (i.e., loudspeaker and L-C low pass filter) connected to the switches can be driven in a push-pull fashion. In such configuration, the load is connected to multiple H-bridge switches such that either zero voltage is applied to both ends of the load or a positive voltage is applied to one end of the load and a negative voltage of equal magnitude is applied to the other end at any given time. In such a configuration, current flowing through the load in one direction represents one positive voltage level; current flowing in the reverse direction represents one negative voltage level; and no current flowing through the load represents the zero voltage level.

Additionally, the control of the magnitude of the outputs of the systems can be achieved by varying the single or multiple voltage levels in concert, which can be accomplished for example by varying a fixed reference voltage level on which all the voltage levels are based.

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The multi-level PWM technique described herein may generally be utilized in other types of systems that generate an analog output from a digital representation. The term analog output should be taken in a broad sense to mean any physical output especially physical output of additive nature which means similar physical outputs can be summed together to form a final physical output e.g. liquid, gaseous, thermal, electromagnetic, or acoustic output etc. Furthermore, the physical output generated from a multi-level electrical signal or by additively combining a plurality of physical outputs (also referred to as analog component outputs) generated from corresponding electrical signals from separate channels or by both multi-level electrical signals and multiple channels whose respective physical outputs are additively combined as disclosed herein shall mean the physical outputs that are converted from their corresponding electrical signals by their converting devices or arrangements. For example, in the digital audio systems, sounds are generated from electrical signals by an arrangement of L-C low pass filters and loudspeakers and in case of liquid outputs, it may mean pumps or fuel injecting devices etc. It will be apparent to those skilled in the art that other modifications to and variations of the disclosed methods and apparatus are possible without departing from the inventive concepts disclosed herein, and therefore the invention should not be viewed as limited except to the full scope and spirit of the appended claims.

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